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REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Subsection (b) of 35 U.S.C. § 132, effective on May 29, 2000,
provides for continued examination of an utility or plant application
filed on or after June 8, 1995.
See The American Inventors Protection Act of 1999 (AIPA).

Application Number	09/843,820
Filing Date	April 30, 2001
First Named Inventor	Takahiko SATO
Group Art Unit	2816
Examiner Name	A. Luu
Attorney Docket Number	108397-00042

#9
8-2502
Payton

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-identified application.

NOTE: 37 C.F.R. § 1.114 is effective on May 29, 2000. If the above-identified application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under 37 C.F.R. § 1.53(d) (PTO/SB/29) instead of a RCE to be eligible for the patent term adjustment provisions of the AIPA. See Changes to application Examination and Provisions Application Practice, Final Rule, 65 Fed. Reg. 50092 (Aug. 16, 2000); Interim Rule, 65 Fed. Reg. 14865 (Mar. 20, 2000), 1233 Off. Gaz. Pat. Office 47 (Apr. 11, 2000), which established RCE practice.

1. Submission required under 37 C.F.R. § 1.114

- a. ☒ Previously submitted
- i. ☒ Consider the amendment(s)/reply under 37 C.F.R. § 1.116 previously filed on July 10, 2002
(Any unentered amendment(s) referred to above will be entered).
- ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- iii. ☐ Other: _____
- b. ☒ Enclosed
- i. ☒ Preliminary Amendment/Reply
- ii. ☐ Affidavit(s)/Declaration(s)
- iii. ☐ Information Disclosure Statement (IDS)
- iv. ☒ Other: _____

2. Miscellaneous

- a. ☐ Suspension of action on the above-identified application is requested under 37 C.F.R. § 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 C.F.R. § 1.17(i) required)
- b. ☐ Other: _____

3. Fees

The RCE fee under 37 C.F.R. § 1.17(e) is required by 37 C.F.R. § 1.114 when the RCE is filed.

- a. ☒ The Director is hereby authorized to charge any deficiency in the following fees or credit any overpayments to Deposit Account No. 01-2300, referencing 108397-00042
- i. ☒ RCE fee required under 37 C.F.R. § 1.17(e)
- ii. ☒ Extension of time fee (37 C.F.R. §§ 1.136 and 1.17)
- iii. ☐ Other: _____
- b. ☒ Check No. 345146 in the amount of \$1140.00.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print/Type)	Lynne D. Anderson	Registration No. (Attorney/Agent)	46,412
Signature	<i>Lynne D. Anderson</i>	Date	August 19, 2002

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner For Patents, Box RCE, Washington, DC 20231, or facsimile transmitted to the U.S. Patent and Trademark Office on:

Name (Print/Type)		Date	
Signature			

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND Fees and Completed Forms to the following address: Assistant Commissioner for Patents, Box RCE, Washington, DC 20231.

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

SATO

Attorney Docket No: 108397-00042

Serial Number: 09/843,820

Group Art Unit: 2816

Filed: April 30, 2001

Examiner: A. Luu

For: SEMICONDUCTOR INTEGRATED CIRCUIT

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#10/C
8-23-02
Payton

PRELIMINARY AMENDMENT WITH FILING OF RCE

Commissioner for Patents
Washington, D.C. 20231

August 19, 2002

Sir:

Prior to continued examination of the above-identified patent application, please amend the application as follows:

IN THE CLAIMS:

Please add claims 10-13 as follows:

--10. (New) The semiconductor integrated circuit according to claims 3, wherein said power-on resetting circuit and said voltage generator include transistors formed through a same manufacturing process.

11. (New) The semiconductor integrated circuit according to claim 10, wherein said transistors are nMOS transistors that have same threshold voltages.

12. (New) The semiconductor integrated circuit according to claims 7, wherein said power-on resetting circuit and said voltage generator include transistors formed through a same manufacturing process.

13. (New) The semiconductor integrated circuit according to claim 12, wherein said transistors are nMOS transistors that have same threshold voltages.--